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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/602,422	06/23/2000	Subramanian S. Meiyappan	VLSI-3505	1374

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EXAMINER	
WHITMORE, STACY	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/602,422	Applicant(s) MEIYAPPAN ET AL.
	Examiner Stacy A Whitmore	Art Unit 2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6, and 8-15* is/are allowed.

6)☒ Claim(s) *16-22* is/are rejected.

7)☒ Claim(s) *9-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL ACTION

Claim Objections

1. Claims 9-15 are objected to because of the following informalities:

I. Claim 9 discloses creating an underlying structure list and performing iterations required to generate an underlying structure list. The claim language is unclear as to whether or not one or two underlying structure lists are created/generated. Also, the parameter application process is claimed as separate, however, the creation and generation of the underlying structure list is done by the parameter application process [as disclosed by applicant on page 20 of the specification. It appears the creation and generation steps are part of the parameter application process].

II. Claims 10-15 also have similar claim limitations related to the modules that perform the functions that are unclear as to the relation between the method steps in the claim language.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (US Patent 5,841,663) in view of Knapp et al. (US Patent 6,370,493).

3. As for claims 16-19, and 21, Sharma disclosed the invention substantially as claimed, including a system on a chip netlist builder and verification computer method comprising the steps of:

receiving system specification information [col. 2, lines 15-19];

reusing standardized circuit block information [47-49, especially pre-defined library modules];

performing test bench integration [];

synthesizing circuit blocks, after proposed circuit design passes the test [col. 2, lines 29-31]; and

creating a top level netlist [col. 2, lines 25-26].

Sharma did not specifically disclose performing test bench integration and [claim 18] writing a test.

Knapp disclosed test bench integration and [claim 18] writing a test [col. 2, lines 27-33; Knapp use of test bench with the simulator is read as a test bench integration; the test bench is a group of instructions in a program which are written].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Sharma and Knapp because Sharma disclosed the use of simulation and verification which would benefit from Knapp's use of a test bench which could be used by Sharma's system to set up simulator to check the HDL descriptions for errors by verifying certain results of the simulation [see Knapp, col. 2, lines 27-33; and Sharma, col. 2, lines 27-30].

Furthermore it would have be obvious to one of ordinary skill in the art at the time the invention was made to write a test because Sharma discloses both simulation and verification which would use a test written for the purpose of verifying circuit design.

4. [claim 17] receiving information associated with custom designed circuit blocks [see Sharma; col. 2, lines 47-50; col. 18, lines 52-53].

5. [claim 19] facilitating communications from a user regarding circuit block selection and parameterization [col. 2, lines 35-50; and col. 18, lines 52-67].

6. [claim 21] retrieving appropriate information from storage sources [col. 2, "HDL modules are stored in a library which inherently includes retrieving appropriate information for a storage source since the modules are used in a computer program which has to retrieve them for design purposes].

7. Claims 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (US Patent 5,841,663) in view of Knapp et al. (US Patent 6,370,493), and further in view of Southgate (US Patent 6,311,309).

8. As for claim 20, Sharma in view of Knapp disclosed the invention substantially as disclosed, including the method of circuit design including the entering of circuit design specification information through a user interface e.g. a text editor [see as cited in the rejection of claim 16; and also see Sharma, col. 3, lines 35-36].

Sharma in view of Knapp did not specifically disclose wherein system specification information is received via a present invention graphical user interface (GUI).

Southgate disclosed receiving system specification information is received via a present invention graphical user interface (GUI) [col. 6, line 62 – col. 7, line 6].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Sharma in view of Knapp, and Southgate because Sharma, Knapp, and Southgate disclose the entering of system specification information about a circuit description which would benefit by the use of a GUI by

making the design parameters entered by a user easier to use than a text based editor and visually informative to the user.

9. As for claim 22, Sharma in view of Knapp disclosed the invention substantially as disclosed, including the method of circuit design including the entering of circuit design specification information through a user interface e.g. a text editor and further HDL design [see as cited in the rejection of claim 16; and also see Sharma, col. 3, lines 35-36; and Sharma; abstract].

Sharma in view of Knapp did not specifically disclose generating HDL files describing connections between building block circuit descriptions and creating external input and output HDL files.

Southgate disclosed generating HDL files describing connections between building block circuit descriptions and creating external input and output HDL files [col. 2, lines 57-63].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Sharma in view of Knapp, and Southgate because Sharma, Knapp, and Southgate disclose simulation of HDL modules as cited above in the rejections of claims 16 and 20 which utilize HDL files for simulation of complex integrated circuits with multiple modules [see Sharma, col. 3, lines 32-33]. Adding Southgate's HDL representations describing the connections of building blocks and external I/O files would provide a way of simulating and verifying the complex interconnected elements of Sharma in view of Knapp's circuit

10. Claims 1-6, and 8-15 are allowable over the prior art of record.

11. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

12. Applicant's arguments with respect to claims 16-22 have been considered but are moot in view of the new ground(s) of rejection.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner
Art Unit 2812

SAW
May 16, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

[redacted]